Kevin Chiaming **Chang**

Ph.D. Candidate | Formal Verification, Control, Machine Learning

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Summary

UC Berkeley Ph.D. candidate developing formal-verification methods for learning-enabled control and hardware systems. Builds solver-backed algorithms that make neural controllers more interpretable and compositional, with research spanning exact controller transformation, contract-based safety analysis, optimization, and CPU microarchitecture verification.

Education

University of California, Berkeley — *Berkeley, CA*

Ph.D. in Electrical and Computer Engineering (GPA: 3.91/4.00) — *01/2021 – Present*

- Research focus: formal verification, learning-enabled cyber-physical systems, optimization, and contract-based design
- Advisor: Prof. Pierluigi Nuzzo; DesCyPhy Lab, Donald O. Pederson Center for Electronic Systems Design

National Taiwan University — *Taipei, Taiwan*

B.S. in Electrical Engineering (GPA: 3.67/4.00, Last 60: 4.00/4.00) — *09/2015 – 01/2020*

- Coursework in physical design, integrated circuits, computer architecture, machine learning, and deep learning
- Undergraduate research in electronic design automation and optimization

Research Experience

DesCyPhy Lab, Prof. Pierluigi Nuzzo — *Berkeley, CA*

Graduate Student Researcher — *01/2021 – Present*

Equivalent Neural-Controller Representations

— Developed a **provably exact transformation** from discrete-output ReLU neural controllers to soft decision trees, with automatic pruning of redundant branches.

— Demonstrated verification-time improvements of up to **20x** on MountainCar, CartPole, and CarRacing; resulted in first-author publications in **IEEE TAC (2026)** and **CDC (2023)**.

Compositional Safety for Learning-Enabled CPS

— Introduced robustness contracts that decouple plant dynamics from neural controllers and enable compositional closed-loop safety verification.

— Designed SMT- and MILP-based refinement algorithms to tighten abstraction bounds and synthesize realizable assume-guarantee specifications under bounded uncertainty.

Deep RL Controller Distillation for Verifiability

— Distilled deep-RL policies into compact decision-tree and kernel controllers, improving interpretability and validation while preserving task performance; resulted in an **Allerton 2022 publication**.

Electronic Design Automation Lab, Prof. Yao-Wen Chang — *Taipei, Taiwan*

Undergraduate Researcher — *09/2018 – 02/2020*

Routing and Optimization for EDA Contests

— Implemented a multithreaded detailed-routing engine that handled designs with up to **1M nets** using less than **64 GB** of memory in 10 hours on most benchmarks.

— Built routability-driven global- and system-level FPGA routers; contributed to **2nd place at ACM ISPD 2019**, a **Top 5 / Honorable Mention at ICCAD 2019**, and an **ICCAD 2021 publication**.

Institute of Information Science, Academia Sinica — *Taipei, Taiwan*

Software Researcher — *06/2018 – 09/2018*

— Implemented a semi-supervised domain-adaptation pipeline for semantic segmentation using unpaired image translation.

— Improved mean IoU on the Cityscapes benchmark by augmenting segmentation training with CycleGAN-generated domain information.

Skills

Research	Formal verification, learning-enabled control, contract-based design, interpretable ML
Methods	SMT, MILP, assume-guarantee reasoning, symbolic abstraction, reachability analysis
Languages	Python, SystemVerilog, MATLAB, C++
Software	PyTorch, scikit-learn, JasperGold, Xcelium, Genus, VCS, Gurobi, CVX

Engineering Experience

Apple — *Cupertino, CA*

Formal Verification Engineer Intern — *05/2026 – 08/2026*

- Developed and debugged **formal properties** for CPU microarchitecture control flow; diagnosed proof failures by refining assertions, assumptions, and coverage targets to distinguish design defects from underconstrained environments.

Teaching Experience

University of California, Berkeley *Berkeley, CA*
Graduate Student Instructor, Introduction to Design Automation *01/2026 – 05/2026*
— Developed end-to-end examples spanning RTL design, simulation, synthesis, timing analysis, and verification; supported students using industry EDA tools.

University of Southern California *Los Angeles, CA*
Graduate Student Instructor, Computer Architecture (3 semesters) *01/2022 – 05/2023*
— Developed examples and guided students through processor pipelines, out-of-order execution, hazards, caching, memory hierarchies, and performance tradeoffs.

Selected Technical Projects

Fantasy Football Performance Prediction *[Python/PyTorch/Scikit-Learn]*
Course Project, Pattern, Prediction, and Action *12/2025*
- Modeled weekly and season-long NFL player performance by combining box-score statistics, expert rankings, and qualitative commentary.
- Built a unified supervised-learning dataset and text embeddings to capture predictive signals beyond structured numerical features.

Physical-Design Algorithm Engines *[C++/Boost]*
Course Projects, Physical Design for Nanometer ICs *04/2019 – 05/2019*
- Implemented a fixed-outline macro floorplanner using a B*-tree representation and simulated annealing.
- Built a Fiduccia–Mattheyses hypergraph partitioner with gain-bucket updates for efficient module moves.

Emergency Exit Guidance System *[Python/PyTorch/Scikit-Learn]*
MakeNTU Hackathon *03/2019*
- Built an object-detection prototype that recommended evacuation directions based on estimated survival probability.

Decentralized Shopping Platform *[Solidity/Web3.js]*
Dexon Hackathon *01/2019*
- Developed an Ethereum marketplace with customer reputation checks and third-party payment support.

Sign Language Translation System *[C++/Python/PyTorch/Scikit-Learn]*
Arm Design Contest *09/2018*
- Built a real-time embedded sign-language translation system using a single 9-DOF IMU for gesture recognition.
- Integrated sensor processing and a learned gesture classifier in a live demonstration; won **2nd Place** and the **Best Popularity Award** among 130+ teams.

FPGA Area-Measurement Vehicle *[SystemVerilog/C++]*
Digital Circuits and Systems Laboratory *02/2018*
- Built an FPGA-based line-tracing vehicle that used a 9-DOF IMU to calculate the area enclosed by its route.

Selected Publications

1. Kevin Chang, Nathan Dahlin, Rahul Jain, and Pierluigi Nuzzo, "Equivalent and Compact Representations of Neural Network Controllers With Decision Trees," *IEEE Transactions on Automatic Control*, 2026, doi: 10.1109/TAC.2026.3676368.
2. Jair Certorio, Kevin Chang, Nuno C. Martins, Pierluigi Nuzzo, and Yasser Shoukry, "Passivity Tools for Hybrid Learning Rules in Large Populations," *Automatica*, vol. 187, Art. 112850, 2026.
3. Kevin Chang, Nathan Dahlin, Rahul Jain, and Pierluigi Nuzzo, "Exact and Cost-Effective Automated Transformation of Neural Network Controllers to Decision Tree Controllers," in *Proc. IEEE Conference on Decision and Control (CDC)*, pp. 7843–7848, 2023.
4. Nathan Dahlin, Kevin Chang, K. C. Kalagarla, Rahul Jain, and Pierluigi Nuzzo, "Practical Control Design for the Deep Learning Age: Distillation of Deep RL-Based Controllers," in *Proc. Allerton Conference on Communication, Control, and Computing*, 2022.
5. Wei-Kai Liu, Ming-Hung Chen, Chiaming Chang, Chen-Chia Chang, and Yao-Wen Chang, "Time-Division Multiplexing Based System-Level FPGA Routing," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2021.

Selected Awards

Outstanding Performance Scholarship, *National Taiwan University* *Taipei, Taiwan*
Awarded for outstanding academic performance in electrical engineering *11/2019*
- Recognized for strong academic performance and undergraduate research contributions.

Top 5 and Honorable Mentions, *Cad Contest Problem C* *Westminster, USA*
LEF/DEF-based open-source global router *11/2019*
- Recognized in an ACM/IEEE contest field of 100+ teams.

2nd Place, *ACM ISPD Contest* *San Francisco, USA*
Initial detailed routing *04/2019*
- Placed 2nd among 33 international teams.

2nd Place and Best Popularity Award, *Arm Design Contest* *Taipei, Taiwan*
Sign language translation system *11/2018*
- Placed in the top 3 among 130+ hardware and embedded-systems teams.